Analogue/Digital Dual Power Module Using Ion-Implanted GaAs MESFETs

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ABSTRACT

An analogue and digital dual power module using ion-implanted GaAs MESFETs with high breakdown voltage has been developed for North American Digital Cellular (NADC). In the analogue operation, the module exhibited high power-added efficiency (PAE) of 56.0% at Vdd=3.7V. In the digital operation, the high efficiency of 46.9% and the low adjacent channel leakage power (Padj) of -29.1dBc at +30kHz Padj and of -52.7dBc at +60kHz Padj were simultaneously obtained at f=836.5MHz, Pout=31.0dBm and Vdd=4.7V. This device is quite suitable for the dual mode application.

INTRODUCTION

In recent years, there has been increasing of the demand of GaAs power MESFETs for analogue and digital cellulars with the spread of them. Since the requirement for a digital power device differs from that for an analogue power device[1)-7)], they have been developed individually. To obtain low distortion properties for digital cellular, which suppress adjacent channel leakage power (Padj), an input signal has to be amplified in a linear region of MESFETs. Moreover, high breakdown voltage require especially for the digital use as compared with the analogue use, because a gate leakage current of MESFETs degrade the distortion properties. In the analogue operation, the input signal has to be amplified in the saturation region of MESFETs to achieve a high efficiency. However, there is no MESFETs by ion-implantation to meet with the needs of the dual mode usage (analogue and digital common use). Furthermore, until now there is no report of the digital power MESFETs that fabricated by ion-implantation. We have realized the newly-developed high breakdown voltage GaAs power MESFETs by ion-implantation, and fabricated an analogue/digital dual power module for North American Digital Cellular (NADC), and achieved a high efficiency and low distortion characteristics in both the analogue and the digital operations.

PROCESS AND DEVICE PERFORMANCES

GaAs power MESFETs were formed by Si ion-implantation. Figure 1 shows the cross-sectional view of the power MESFET. An active layer of MESFET was implanted at 80keV with dosage of 3.9×10^{12} cm^{-2} and was activated by $WSiN/SiO_2$ capped annealing method[8)]. An annealing was performed at 820°C in an Ar/H_2 atmosphere. This technique keeps a high peak carrier concentration without deep tailing of a carrier concentration profile after annealing, which achieved high transconductance. An offset gate structure was adopted to reduce a source resistance, which are essential for high efficiency and low operating voltage[9),10)]. Recess etching process with aluminum gate and a novel dry etching technique realized high drain-gate breakdown voltage (BVgd) of over 15V. A typical drain saturation current (Idss), threshold voltage (Vth) and transconductance (gm) are about 170mA/mm, -2.5V and 65mS/mm, respectively.

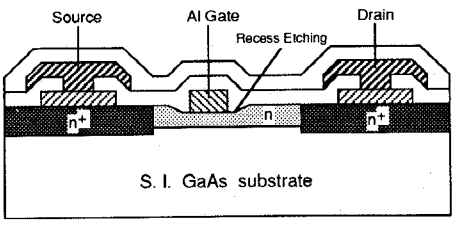

Figure 1 Cross-sectional view of GaAs power MESFET.

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RF characteristics were measured in order to optimize device dimensions of FETs. We have investigated the relations between Padj and gate-width (Wg) or gate-length (Lg) of the FETs in the digital operation. An input signal is π/4-shift DQPSK, and RF measurement was performed under the Personal Digital Cellular (PDC) standard of Japanese digital cellular phone. A supply voltage and an operating frequency are 4.7V and 948MHz, respectively. A gate bias was supplied through breeder resistors, and an idle current was fixed at the value of 400mA. MESFETs were evaluated by using a matching circuit formed on a printed board. Matching circuits were optimized on conditions of Padj<-50dBc at Pout=31.0dBm for each device. Figure 2 shows the gate-width dependence of -50kHz Padj, where the gate-length is 1μm. Padj of the wide gate-width FET exhibited low distortion characteristics at the higher output power region as compared with that of the narrow gate width FET. Padj of the 24mm gate-width FET had no margin for the PDC standard at the higher output power region (Pout>31.5dBm). At Pout=31.0dBm, gain decreased with increasing of gate-width, and 30mm gate-width FET showed the maximum PAE of 48% with gain of 10.5dB. The gate-length dependence of 30mm gate-width FET is shown in Figure 3. It was clearly showed that Padj of 0.6μm gate-length FET was worse than that of 1.0μm gate-length FET in the output power region of less than 32dBm. It's because the drain conductance (gd) of 0.6μm gate-length FET is lower than that of 1.0μm gate-length FET. RF characteristics of 0.6μm gate-length FET showed higher gain of 10.62dB and lower PAE of 38.9% as compared with those of 1.0μm gate-length FET at Pout=31dBm. Meanwhile gain and PAE of 1.4μm gate-length FET were 9.1dB and 41.4%, respectively. From these results, we have chosen the 30mm gate-width FET with the 1μm gate-length as the 2nd-stage FET.

Figure 4 shows the relations of ΔIg and ±50kHz Padj. ΔIg is defined as the difference between an initial gate current and a gate current during RF operation. It is equal to the gate leakage current and consequently correspond to the drain-gate breakdown voltage. With increasing of ΔIg, an asymmetry of ±50kHz Padj became larger. Two reasons were considered about it : (1) the FETs were miss-matched to the circuit by changing the gate bias through the breeder resistors, (2) the phase rotation increased with the gate leakage current[2]. But further study is necessary to understand the mechanism. From this result, it is clear that low leakage current and consequently

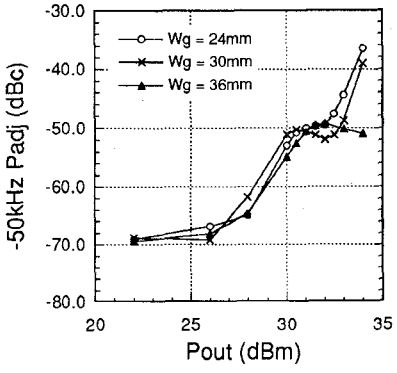

Figure 2 Gate-width dependence of adjacent channel leakage power (Padj) of 1μm gate-length GaAs MESFET at Vdd=4.7V.
input signal : f=948MHz, π/4-shift DQPSK modulation
Padj : at 50kHz apart from 948MHz

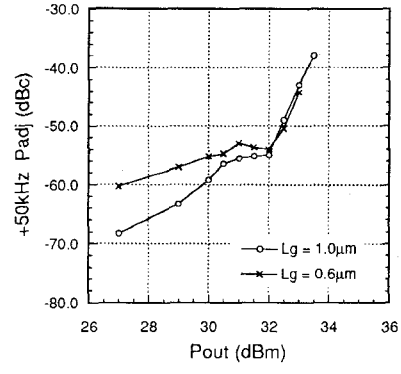

Figure 3 Gate-length dependence of 30mm gate-width GaAs MESFET in the digital RF characteristics at Vdd=4.7V.
input signal : f=948MHz, π/4-shift DQPSK modulation
Padj : at 50kHz apart from 948MHz

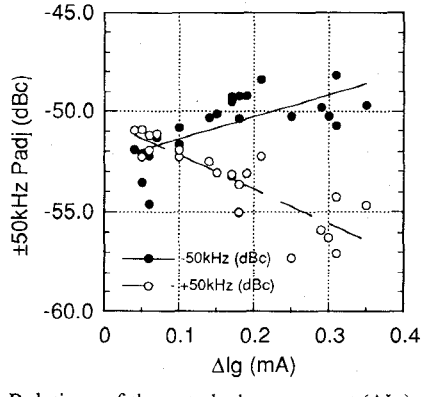

Figure 4 Relations of the gate leakage current (ΔIg) and ±50kHz adjacent channel leakage power (Padj) of 30mm gate-width GaAs MESFET at Pout=31.0dBm and Vdd=4.7V.
input signal : f=948MHz, π/4-shift DQPSK modulation
Padj : at 50kHz apart from 948MHz

high drain-gate breakdown voltage are essential to digital application.

We have measured total RF characteristics of GaAs MESFET with the gate-width of 30mm and the gate-length of 1.0μm for the application to the NADC dual mode. Figure 5 is the photograph of the GaAs power MESFET. The chip size is 2.1mm x 0.65mm. The operating frequency is 836.5MHz. RF measurement was performed under the NADC standard. At Pout=31.0dBm, the FET showed high power added efficiency (PAE) of 59.0% in the analogue operation at Vdd=3.7V, and the PAE of 49.6% and the low Padj of -30.1dBc for +30kHz Padj and -54.4dBc for +60kHz Padj apart from the center frequency in the digital operation at Vdd=4.7V.

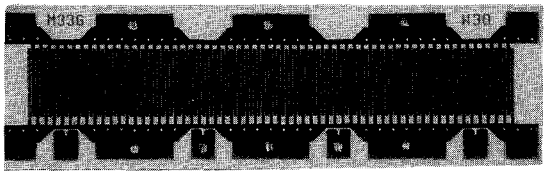

Figure 5 GaAs power MESFET with the gate-width of 30mm and the gate-length of 1μm. The chip size is 2.1mm x 0.65mm.

MODULE CHARACTERISTICS

An analogue/digital dual power module has been fabricated for NADC. Figures 6 and 7 are the photograph of the fabricated power module and the equivalent circuit, respectively. The module is composed of 2-stage FETs and an impedance matching circuit. The 1st-stage MESFET has the gate-length of 0.8μm and the gate-width of 6mm. The chip size of the 1st-stage FET is 0.9mm x 0.6mm. The volume and the size of the module are 0.4cc and 13.0mm x 10.6mm, respectively. Load impedance was optimized in order to achieve low distortion without a reduction of PAE at Pout=31dBm. Idle currents were controlled by changing the gate voltage (Vgg) in each operation.

Figure 8 shows the dependence of Pout and PAE on input power (Pin) of the module in the analogue operation, where the operating conditions are as follows, frequency f=836.5MHz and the supply voltage Vdd=3.7V. The idle currents of the 1st-stage FET and the 2nd-stage FET were 20mA and 77mA, respectively. A typical RF data of the module are Pout=31.05dBm and PAE=56.0% at Pin=9dBm.

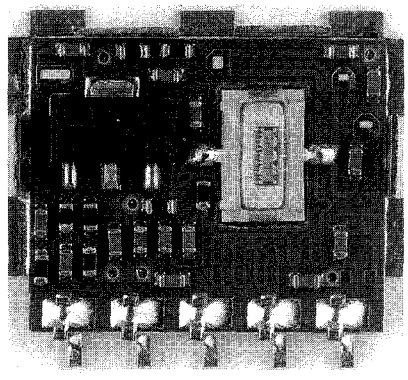

Figure 6 Photograph of the fabricated GaAs power module. The volume and the size of the module are 0.4cc and 13.0mm x 10.6mm, respectively.

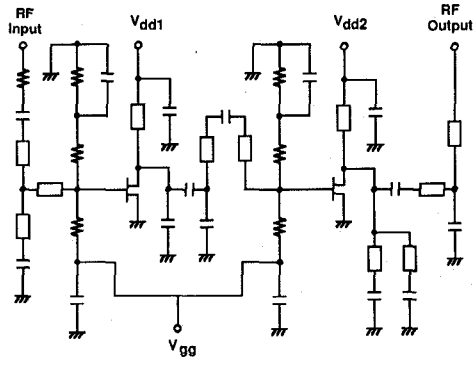

Figure 7 Equivalent circuit of a dual power module.

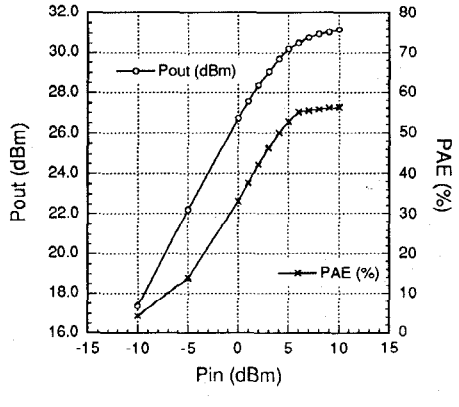

Figure 8 Output power (Pout) and power added efficiency (PAE) of the GaAs power module in the analogue operation at Vdd=3.7V and f=836.5MHz.

Figure 9 shows the relations of Padj and PAE versus Pout in the digital operation. The idle currents were set to be Ids1=76mA and Ids2=400mA, respectively. The high efficiency of 46.9% and the low distortion properties of -29.1dBc for +30kHz Padj and -52.7dBc for +60kHz Padj were obtained with gain=26.8dB at Pout=31dBm and Vdd=4.7V. These results indicate that this device has a great potential for the dual mode operation.

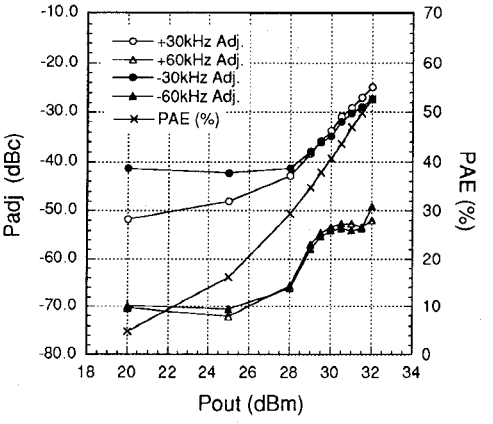

Figure 9 Adjacent channel leakage power (Padj) and power added efficiency (PAE) of the GaAs power module in the digital operation at Vdd=4.7V.
input signal : f=836.5MHz, π/4-shift DQPSK modulation
Padj : at 30kHz and 60kHz apart from 836.5MHz

CONCLUSION

We have developed the low-distortion and high-efficiency analogue/digital dual power module by using ion-implanted GaAs MESFETs with a high breakdown voltage for NADC. The fabricated power module showed excellent RF performances. In the analogue operation, the module exhibited high power added efficiency (PAE) of 56.0% at f=836.5MHz, Pout=31.0dBm and Vdd=3.7V. In the digital operation, the high efficiency of 46.9% and the low adjacent channel leakage power (Padj) of -29.1dBc at +30kHz Padj and of -52.7dBc at +60kHz Padj were obtained at Vdd=4.7V. The developed power MESFETs and module contribute to spreading a dual mode cellular systems such as NADC.

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